REMARKS

I. Introduction

In response to the pending Office Action, Applicants have added new claims 42-51 so as to recite further aspects of the invention not previously claimed. No new matter has been added.

Applicants again note with appreciation the indication of allowance of claims 34-40. Applicants also wish to thank Examiner Warren for his time and courtesy for the interview conducted on July 9, 2003. While a formal agreement was not reached, Examiner Warren tentatively conceded that the cited prior art did not disclose the claimed invention for the reasons set forth below.

II. The Rejection Of Claims 22 and 23 In View Of Nagai

Claims 22 and 23 were rejected under 35 U.S.C. § 102 in view of USP No. 6,114,767 to Nagai. Applicants respectfully submit that claims 22 and 23 are not anticipated by Nagai for at least the following reasons.

As recited by claim 22, the present invention relates to the structure of a basic CMOS cell contained in a gate array integrated circuit having a plurality of such cells. Figs. 1A and 1C illustrate the structure of the basic CMOS cell as recited by claim 22. As shown, the exemplary cell comprises n-channel transistors (TN1 and TN2) and p-channel transistors (TP1 and TP2) and interconnects 53 and 54 connected to the gate

electrode (2A and 2B) of the p-channel transistor TP1 and the n-channel transistor TN1, respectively. In addition, each cell comprises an interconnect pattern, which is identified by reference numeral 9 in Fig. 1A, which is formed in the uppermost interconnect layer of the basic cell (i.e., as shown in Fig. 1F it is possible for the basic cell to comprise multiple layers of interconnections (e.g., 54, 56), the interconnect pattern 9 is formed in the uppermost layer). Importantly, within the basic cell the interconnect pattern 9 is not coupled to the n-channel transistor, the p-channel transistor or the interconnect coupled to the transistors. Thus, the interconnect pattern may be isolated from the contact hole (55 and 56) and interconnect (53 and 54) contained in the basic cell that are coupled to the transistors.

Turning to Nagai, and the pending rejection, it is asserted that Figs. 9 and 11e of Nagai disclose the claimed basic cell, which includes both an N-channel transistor and a P-channel transistor. As explained during the interview, Nagai does not do so. Referring to col. 9, lines 1-16 thereof, Nagai indicates the structure illustrated in the cited figures corresponds to the memory cell structure, not the CMOS structure. As stated in this section, the ***memory cell structure*** which is shown in the figures (i.e., Figs. 9 and 11) causes the CMOS transistors located outside the memory cell regions to have an LDD structure. Indeed, CMOS transistors do not appear to be shown in Nagai. Thus, as Nagai does not disclose the structure of CMOS cells, it is clear that Nagai does not disclose the claimed invention.

The foregoing is confirmed by the fact that the doping of the channel region 2

and the source and drain regions 8a and 8b as shown in Fig. 11 of Nagai all appear to be the same, as described by col. 7, lines 64-66 of Nagai. As a result, Nagai does not disclose N-type and P-type transistors in the figures cited in the pending rejection, and therefore does not disclose the claimed basic cell.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Nagai does not anticipate either claim 22 or 23.

III. The Rejection Of Claim 41 Under 35 U.S.C. § 102

Claim 41 was rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,091,088 to Arima. Applicants respectfully submit that claim 41, as amended, is patentable over Arima.

Referring to Fig. 27a of the specification, claim 41 has been amended to recite that for both of the gates of the n-channel transistors contained in the given cell, the hooked portion 101b, extending in a first direction, of one of the gates is aligned in the "vertical" direction with the hooked portion 104c of the other gate, extending in a second direction. In other words, both of the hooked portions 101b and 104c of the respective gates intersect the vertical line designated by reference numeral V2 in Fig. 27a. Claim 41 has also be amended to recite that the p-channel transistors also exhibit the same

structure, as is shown in Fig. 27a.

Turning to Arima, it is clear that Arima fails to disclose this element of amended claim 41. While Arima does disclose gate electrodes have bent portions, it is also clear that the bent portions of the gate electrode of Arima do not align along a vertical axis as recited by claim 41.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Arima does not anticipate claim 41.

IV. Dependent Claims 24-33 Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 22 is patentable for the reasons set forth above, it is respectfully submitted that claims 24-33 are also in condition for allowance.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417.

Respectfully submitted,

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